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Adaptation of counters redundant bits with the provision of dual supply and modified clock gating to favour of low power in VLSI

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The utilization of usual supply voltage and clock for repetitive state transistors in digital circuits is a fundamental driver for high power utilization. Most significant bit states of the counter stay longer than the least significant bit states and it has some repetitive states. To limit the supply voltage and stop the clock for MSB Flip Flop (FF) transistor, our method uses Control Combinational Logic, Voltage selector and Modified Integrated Clock Gating blocks. The LSB transistor always have a supply voltage of 1.2V and succession of the clock, while MSB transistor gets just 480mV and the clock will be stopped by the this technique. Bring down the supply voltage and quit the clock for redundant states either 0 or 1 in MSB. Meantime supply 1.2V and clock for state changes over from one state to next state. The experimental simulation was done in 45nm CMOS technology using Cadence virtuoso indicates that this asynchronous counter achieves a power savings of 23.57% and the same modified technique when applied to the counters with transmission-gate FF, hybrid-latch FF and sense amplifier FF will have more than 40% power savings and the technique applied in some benchmark circuits will have more than 22% power savings than existing techniques.

Keywords: Control Combinational Logic, Voltage Selector, Modified Clock Gating, Low Power, Counter

1 Introduction

In integrated circuits dynamic power is relative to the square of the supply voltage. The most perceptible parameter to reduce the dynamic power[1] is supply voltage[2-4]. So, this method focuses on supply voltage and clock to reduce the power dissipation 16-bit asynchronous counter[5]. Leakage currents are particularly essential in blasted mode type incorporated circuits where most of the time the framework is in an inert, or rest mode where no calculation is occurring. For instance, in a mobile phone a terminal will spend more than 90% of the time in a standby mode, where the processor is hanging tight for client input. For this class of burst-mode-type applications, it might be acceptable to have expansive leakage current long with the dynamic mode. However, it is extremely inefficient to have vast leakage current[6] along with the idle state since power will be ceaselessly depleted with related work being done. There have been a few reported strategies to help reduce sub-threshold leakage current along with backup modes. Examples include using the stack impact, where one can reduce sub-edge leakages by compelling arrangement transistors to be simultaneously off or utilizing reverse body biasing to increment threshold voltages[7]. Be that as it may, the stack impact just gives limited reduction over leakage current, and body biasing effectiveness reduces with innovation scaling. Another methodology that can be quite powerful at controlling sub-threshold leakage current is to utilize double edge voltage innovation[8]. Multipurpose electronic devices can be used to diminish leakage current while low gadgets can be used at points superiority is required. The most straight-forward use of double innovation is basically to partitioned circuit into basic and noncritical locales, and to possibly utilize fast low-gadgets when it is important to meet execution objectives. This approach will diminish sub-threshold leakage current[6, 9] both in the dynamic mode and the reserve mode, however leakage decrease may be limited if the circuit contains numerous basic ways. The rest of this paper will investigate two other double edge voltage circuits' styles for diminishing backup leakage current in combinational logic circuits. In a 16-bit counter above causes occurred due to frequent supply of voltage[10]

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and clock[11-12] for repeated states produced the same transistors. This kind of transistors only induces the Leakage and dynamic dissipation[13]. In the modified circuit controls both the issues by Control Combinational Logic (CCL), Voltage Selector and Modified Integrated Clock Gating (MICG) in Fig.1.

Existing circuits and their restrictions are discussed in section II. The modified technique and their blocks operation through simulation using cadence 45nm CMOS technology such as CCL, VS and MICG (combination of inverter and ICG) are discussed in section III. Discuss the Experimental result by cadence virtuoso in section IV and Final result conclusion in section V.

2 Existing methods and their limitations

Conventional dual voltage supply method[1-2, 14] put low voltage gates on the noncritical paths and high voltage gates on the critical paths, this will reduce the energy consumption in the low voltage gates. Other than adaptive supply voltage (ASV), adaptive body bias (ABB) [15-16] is another notable versatile system. The existing method of ABB decreases the transistor junction voltage to restore execution or increment the limit voltage to decrease leakage control. ASV has a few focal points over ABB. To start with, ASV can be connected to practically any sort of circuits, while ABB is hard to be connected on Silicon-on-Insulator (SOI) circuits. Second, the tuning scope of ABB is constrained due to intersection leakage current[15].

Third, ABB influences just leakage control, while ASV can change both leakage power and dynamic power. Meanwhile, Dual ASV technique avoids the Power routing overhead than the other two, but it is limited to voltage island-based designs. Multi-threshold CMOS (MTCMOS) is a double technology that is compelling at diminishing leakage current in the standby mode. This procedure incorporates using high-transistors to gate the control supplies of a low-basis deter as showed up. When the high-transistors are turned on, the low-logic is associated with virtual ground and power, and exchanging is performed through quick gadgets. Genuine disadvantages to the boundless utilization of MTCMOS are that fitting rest transistor measuring turns out to be troublesome and those consecutive circuits will lose information[17] when the power transistors are turned off. The above conventional methods drawbacks of quiescent power consumption; low threshold voltage problem can be avoided by the modified technique. This method passes 480mV to MSB transistor and holds the data without loss. In the cut off region (Vgs-Vt),

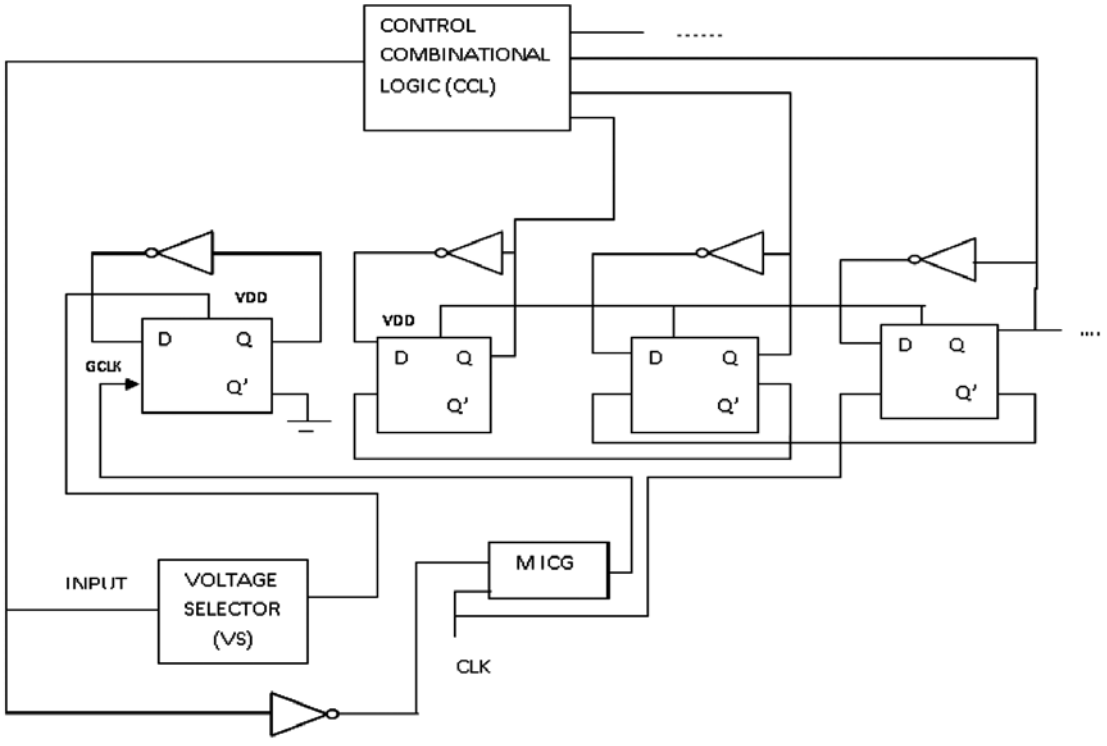

Fig. 1 — Modified Architecture.

transistor[18] will consume little power from the source which results in lesser leakage current. Most of the time delay induces the leakage and pulls down the circuit performance[6]. So, researchers use a switch level simulator to calculate the delay in circuits. Redundant switching activity and load capacitance will increase the power consumption. To overcome these issues our method concentrates on switching delay and leakages[3, 19].The Clock frequency is the main factor for high power consumption[20] in order to reduce the power consumption, minimize the clock frequency and uses fault-tolerant circuits[21-22]. Low threshold voltage[7] increases the performance but decreases the low power device operation. Passing the minimum voltage of 480mV to the redundant transistor in 16-bit ripple counter to avoid the above factors and neglect the skew in the circuits is presented. To avoid the skew, information bit must be available before the clock recurrence[14, 16,18]. If unexpected shut down of supply to the counter states, it cannot lap with clock at a time. To avoid this mismatching (which creates the leakage), maintain the states with a minimum supply voltage of 480mV. For the modified technique dual supply 1.2V and 480mV passed by Voltage selector(VS) with the help of Control Combinational Logic(CCL) which is shown in Fig. 1.

q In this paper two methods have been presented to attain the Low power in digital circuits. Main think of the approach can be summarized as follows.

i. MICGout cut the clock for redundant states occurred in Most Significant Bit (MSB) of D15 State.
ii. VSout reduce the power supply from1.2V to 480mV and pass to the redundant states, which is occurred in MSB.
iii. This above two parallel processes will reduce the power consumption, cut the delay and minimize the skew which is dominantly appeared in existing method.

3 Modified Technique

The 16-bit ripple counter delivering the all conceivable of states, in that part of repetitive state likewise will devour the voltage and clock flag. This superfluous supply voltage and clock for the excess state[23] will stop by this Logic, for example, CCL, VS

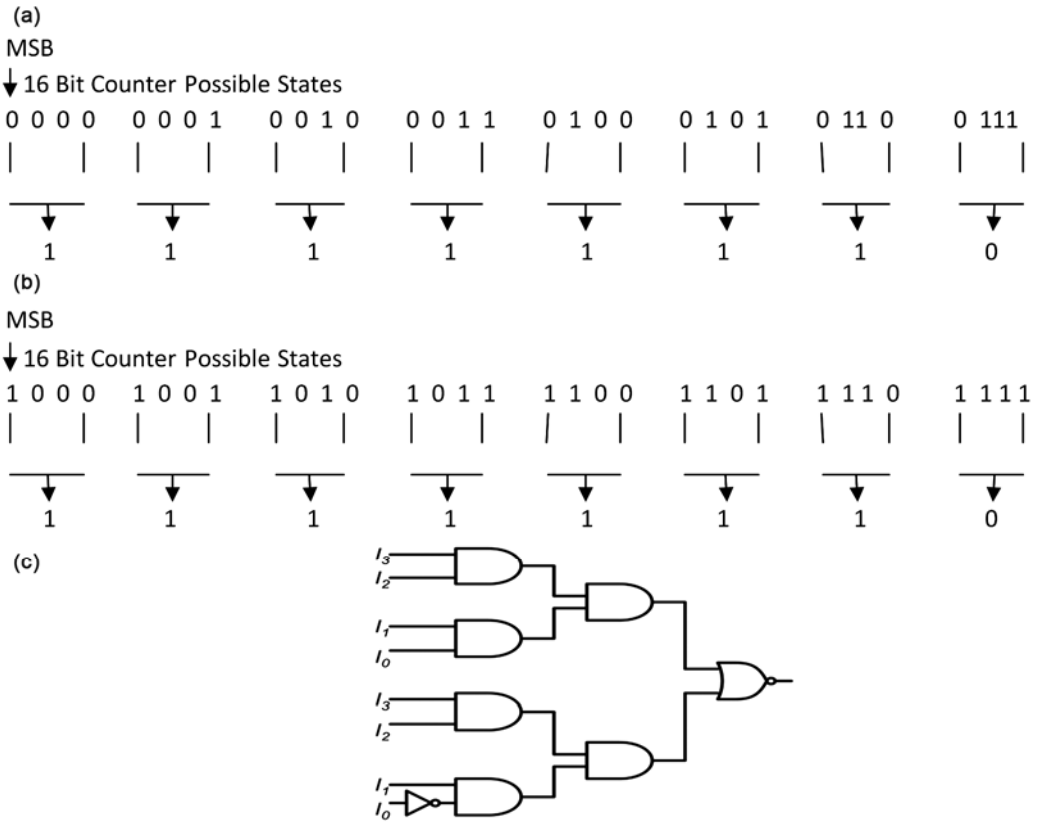

Fig. 2 — Modified CCL Conditional Bit Sequence (a) Redundant MSB is Zero (b) Redundant MSB is one (c) CCL RTL Schematic.

and MICG. The 16-bit counter and our proposed output associations appeared in Fig. 2. Basically, higher-order bit stays longer than lower-order bit in Fig. 2 a-b. In this regard, MSB is in standby mode and periodically consumes the power. This power ignore is handled by the modified technique. From the Fig. 2 the operation of CCL for 16-bit Counter States and produce the outputs, which is the control input to Voltage Selector (VS) and Modified Integrated Clock Gating (MICG). Each 4-bit States of 16-bit Counter give as input to the CCL and produce the Consolidated single bit output. The modified CCL produce Logic 1 for counter states 0000 to 0110 and produce Logic 0 for state of 0111.Since MSB state change from 0 to 1 & LSB states are changed from 1 to 0. Likewise, CCL in Fig. 2(c) produce Logic 1 for counter states 1000 to 1110 and produce Logic 0 for state of 1111.Since MSB state change from 1 to 0 & LSB states are changed to ZERO. The power reduction technique by minimized supply voltage of combinational equation is as follows.

$$Power_{optimized}\,Counterstategeneration = D_0V_{1.2v} + D_1V_{1.2v} + \cdots + \underbrace{D_{15}VS_{480mV}}_{\substack{Power\ optimized\ state\\ by\ stop\ unnecessary\\ of\ high\ voltage}} \quad \ldots (1)$$

The output of the CCL goes to the VS block, in which either 1.2V or 480mV is chosen to be given to the repetitive MSB transistor Fig. 3. At the point when a group of the CCL produces logic 1 for the combination of possible inputs 0000-0110 except 0111.Likewise, a group of the CCL produces logic 1 for the combination of possible inputs 1000-1110 except 1111.For the above conditional inputs VS choose the particular voltage either 1.2V or 480mVfor power utilization for 16-bit ripple counter. The schematic of Voltage Selector (VS) in Fig. 3 is built by NMOS and PMOS. Gates of both transistors are connected to the output of the CCL. At the point when input is logic 1 to the voltage selector NMOS transistor will turn ON, it chooses 480mV as supply to the redundant MSB transistor. Giving this minimum voltage rather than cut the voltage for redundant transistor is to keep away from quiescent power consumption and maintain strategic distance from skew. Abrupt charging from the discharged capacitor induces the delay and incites the skew. For contact of transistor need enough time and it should ignore the threshold value, because before threshold value it will be inert stage. The conditional equation (1) will explain the supply voltage such as 1.2V and 480mVfor counter states transistor. It is clearly explained, which most significant bit transistor (D15) have redundant bits, modified voltage selector (VS) generate 480mV to that particular transistor remain transistors (D0-D14) will operate with 1.2V.When the input is logic 0 to the voltage selector PMOS

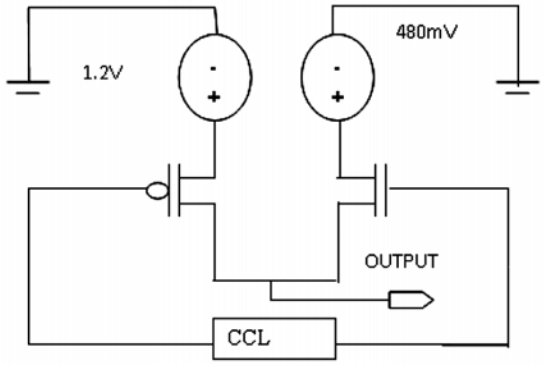

Fig. 3 — Schematic Diagram of modified Voltage Selector.

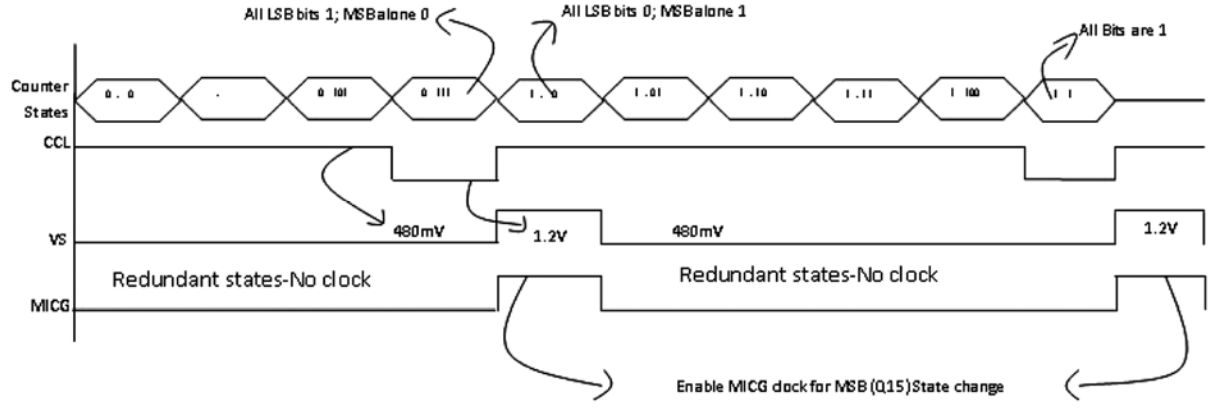

Fig. 4 — Timing Diagram of the modified Ripple Counter.

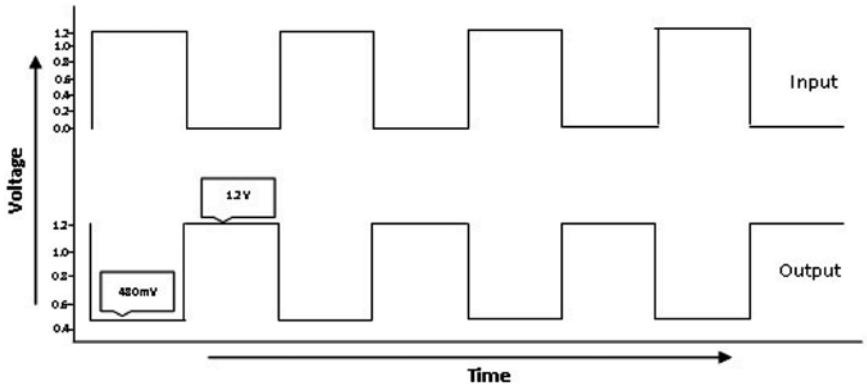

Fig. 5 — Timing Diagram of Voltage selector according to CCL input.

transistor will turn ON, it chooses 1.2V as supply to the LSB transistor. The Timing diagram of Fig. 4 plainly demonstrates the go of 480mV to the redundant MSB state Transistors to spare the power utilization in 16-bit ripple counter. The outputs of the CCL Logic 0 go to the gate of both transistors, for this condition PMOS will turn ON and produce the 1.2V to the LSB transistor in Fig. 5.

The power consumption in LSB transistors is limited by the standard supply voltage. The above Same CCL output logic likewise go to the MICG to cut the complete clock for redundant state MSB Transistor in Fig. 4. The output of the CCL similarly goes to the VS and MICG. Here ICG contains D Flip Flop & AND gate. Regular engage commitment of ICG experienced inverter is called Control Signal (CS).At the point when CCL output logic 1 go to the MICG Fig. 6(a), it will stop the clock for redundant MSB states in 16-bit ripple counter. For at the spot of single input signal (from Group of CCL) drive the VS in Fig. 5 and MICG Fig. 6(a) simultaneously and these devices save the supply voltage & clocks Paralleled. This parallel on-time process will cut the delay and skew which is dominantly appeared in the existing method. For limiting the power in asynchronous ripple counter by quit the clock to excess state delivered MSB transistor (Q15) is determined by the accompanying condition by equation 2.

$$Clock\ Optimized(CLK_{opti})CounterStates\ Generation = D_0CLK + D_1\overline{Q}_0 + D_2\overline{Q}_1 + \cdots + \underbrace{D_{15}MICG_{out}}_{\substack{Power\ optimized\ state \\ by\ stop\ the\ clock}} \quad \ldots(2)$$

This method considers a single bit as Most significant bit (MSB) and remain the bits are considered as Least significant bit (LSB) in 16-bit

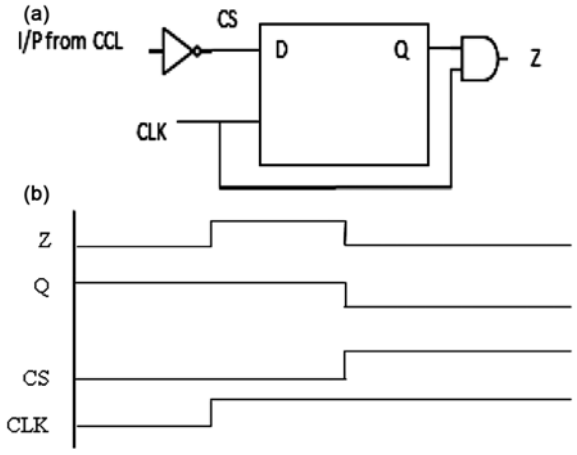

Fig. 6 — MICG (a) Structure (b) Output waveform.

Table 1 —Truth Table for modified methods (CCL, VS and MICG) for Low Power 16-bit Counter

MSB BIT	LSB BITS			Control Combinational Logic (CCL) Output	Voltage Selector (VS) Output	Modified Integrated Clock Gating (MICG) Output
0	0	0	0	1	480mV	No clock
0	0	0	1	1	480mV	No clock
0	0	1	0	1	480mV	No clock
.				1	480mV	No clock
.				1	480mV	No clock
.				1	480mV	No clock
0	1	1	1	0	1.2V	Clock present
1	0	0	0	1	480mV	No clock
.				1	480mV	No clock
.				1	480mV	No clock
.				1	480mV	No clock
1	1	1	1	0	1.2V	Clock present

counter states. Table 1 elaborates on the operation of modified methods such as CCL, VS and MICG. As the reference of Fig. 4 (which is simulated by cadence virtuoso) the 16-bit counter truth table has formed

which is keenly explained the supply voltage and clock for every states. For repeated MSB states such as logic 0 and 1, counter circuits get 480mV and absence of clock signal. Exceptional case of MSB is logic 0 and both LSB are logic 1, counter particular states will get 1.2V and clock signal, which is used to change the state from 0 to 1. Likewise MSB is 1 and both LSB are 1will get 1.2V and clock signal, which is used to change the state from 1 to 0. The clock generating using MICG is in Fig. 6(b).

4 Experimental Result And Analysis

The main experimental results are obtained from cadence virtuoso and Simulation of CCL, MICG obtained by Xilinx vivado. The above logic is actualized in 16-bit ripple counter utilizing Cadence Virtuoso 45 nm technology to investigate the power with the existing outputs. The power breaks down dependent on High VDD and Low VDD for modified technique and existing strategy. For decreasing the power, modified technique has included additional blocks, which may devour the option of intensity. In any case in our work the power utilization is exceptionally less. Since the system decrease the supply voltage and slice the clock to repetitive states. Fig. 7schematic plainly demonstrates the connections of 16-bit ripple counter and modified logic. Their reference block and their output go to the VS just as MICG. These two blocks lessen the voltage and stop the clock to repetitive MSB transistor. The output of the VS is 480mV to the repetitive MSB when it gets Logic 1. When it gets

Logic 0, the output of VS is 1.2V to MSB transistor. Here MICG output depends on the CCL. At the point when MICG gets Logic 1, it will Cut the clock to Redundant MSB transistor and passes the clock for same transistor when MICG gets Logic 0 in Fig. 4. In Fig.4 simulation of redundant state is run by 480mV and no clock passes to the repeated states. Remaining of the states will get the consecutive clocks and regular power supply of 1.2V to state change. Only during state change from 0 to 1 or 1 to 0 MSB transistor needs high clock and voltage of 1.2V while in the remaining period MSB state is run by zero clock and 480mV of power supply. In Fig. 4 before the MSB state changes, all LSB states are 1, as per condition explained in Fig. 2. Simulation of the Fig. 4 using cadence virtuoso has to be discussed as timing diagram, which leads to give 480mV supply and cut the clock for repeated states and supply 1.2V, clock signal for remain states.

The 16-bit ripple counter with & without MICG, supply voltage and their power consumption have been consolidated in Table 2 and Fig. 8.Basic supply voltage of 1.2V in cadence for implementing the 16-bit counter without and with MICG will consume 72µW and 60 µW of power. On adding the dual voltage 1.2V and 480mV by voltage selector and MICG block done the improvement in power consumption is 16.6%. Fig. 9(a) shows the comparative power analysis of existing versus modified techniques, in that Transmission Gate (TG), Hybrid Latch (HL) and Sense Amplifier (SA) based Flip Flop with clock gating[11] and

Table 2 — Power Analysis With respect to VDD,H & VDD,L

Supply Voltage(V)		16 Bit Counter Power (µW) Without MICG	16 Bit Counter Power (µW) With MICG (µW)	Improvement (%)
$V_{DD,H}$	1.2V	72	60	16.6
$V_{DD,H}$ $V_{DD,L}$	1.2V - 480mV	52.6	40.2	23.57

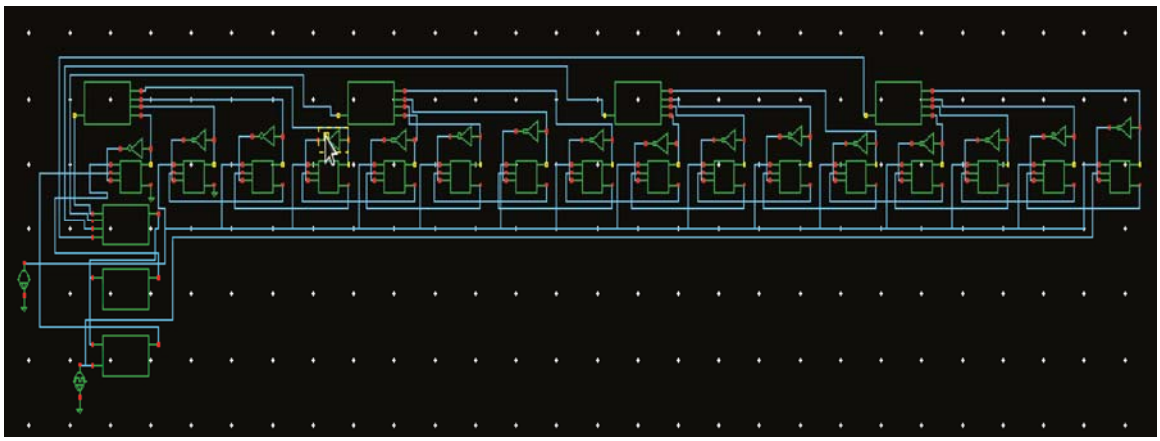

Fig. 7 — Schematic of modified 16-bit ripple counter using cadence virtuoso.

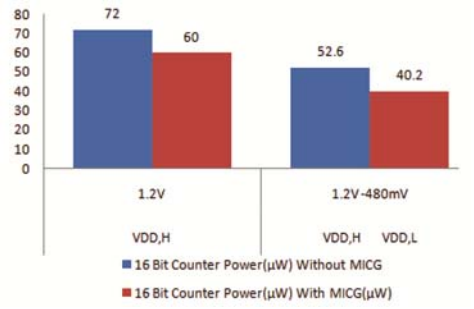

Fig. 8 — Power Analysis for16-bit counter.

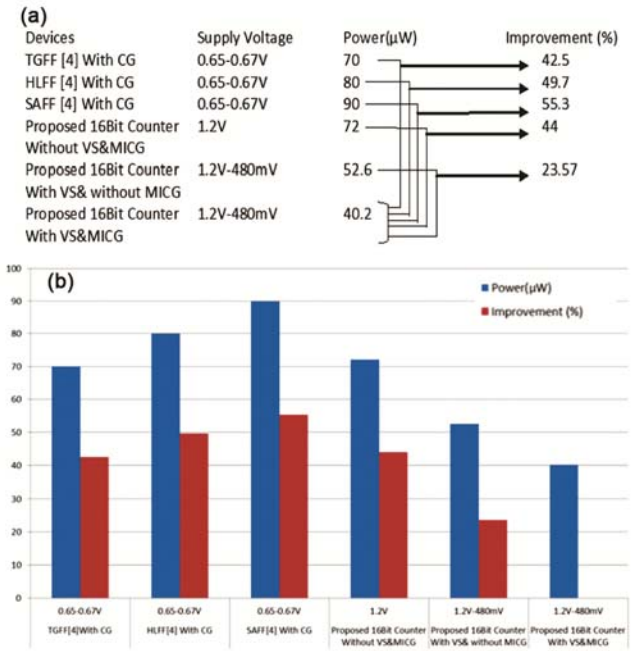

Fig. 9 — Power analysis (a) with the exciting methods (b) comparative analysis of modified with reported work[4].

Table 3 — ISCAS89 Devices[2] Power compare with modified technique

Devices	ASV VDD(V)	Power (mW)	DASV VDD, L(V)	Power (mW)	Modified Technique VDD	Power (mW)
S526	0.78-0.98	2.88	0.70-0.90	2.50	480mV-1.2V	1.88
S5378	0.80-0.95	10.56	0.85-0.95	7.94	480mV-1.2V	5.84

proposed method with VS & without MICG is compared with the modified method with VS & MICG. Here TGFF operating voltage is 0.65-0.67V and their power consumption is 70µW which is 42.5% high power than the proposed technique, meanwhile HLFF and SAFF operating voltages are 0.65-0.67V and their power consumption is 80µW & 90µW. For the same circuits our technique achieved >49% power savings shows in Fig. 9.

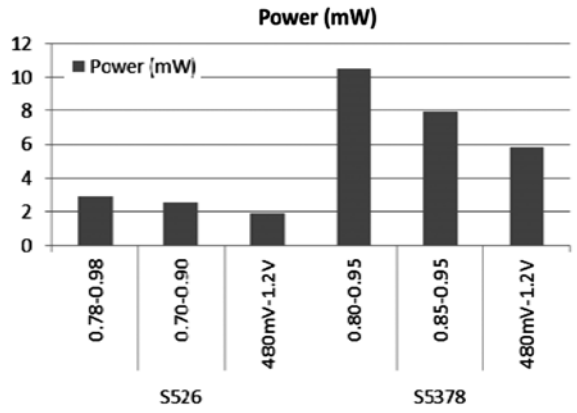

Fig. 10 — Benchmark circuits Power Analysis using various source voltages.

The ISCAS89 devices S526 and S5378 power analysis with ASV, DASV and the modified techniques are consolidated in Table 3 and Fig. 10.The supply voltage of the S526 & S5378 is 0.78V-0.98V & 0.80V-0.95V respectively, for that power consumption is 2.88µW &10.56 µW. This problem already rectified by DASV. So proposed method comparison only is held with DASV, which S526& S5378 uses 0.70V-0.90V & 0.85V-0.95V and their power consumption is 2.50mW & 7.94mW. This high power utilization decreased and improves the ability to 24.8% and 26.44% by the modified strategy.

5 Conclusions

The schematic of 16-bit Ripple counter connected with modified logic, for example, Control Combinational Logic (CCL), Voltage Selector (VS) and Modified Clock Gating (MICG) to lessen the power utilization of about 40% than typical 16 bit ripple counter and existing strategies. Meanwhile the investigation with two techniques like a 16-bit counter with VS and without MICG and a 16-bit counter with VS and MICG will convey the reduced power of 23.57%.The same approach has applied to S526 and S5378 with operating voltage of 480mV-1.2V it is had improvement of 24.8% and 26.44% low power than DASV. Analyze the TGFF with operating voltage of 0.65-0.67V and their power consumption is 70µW which consumes 42.5% high power than the modified technique, meanwhile HLFF and SAFF operating voltages are 0.65-0.67V and their power consumption is 80µW & 90µW, which the circuits consume 49.7% and 55.3% high power than proposed technique.

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